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The diagram illustrates a system architecture. At the top, a large rectangle represents **Memory 201**. Inside this rectangle, a horizontal row of three squares represents a set of tiles. The middle square is labeled **tile 210**. A double-headed arrow above the tiles is labeled **tile width**, and a double-headed arrow to the right of the tiles is labeled **tile height**. A long double-headed arrow below the tiles spans the width of the three tiles and is labeled **image width = line offset**. Below the memory array, a large double-headed vertical arrow connects it to a block labeled **WAVELET PROCESSING LOGIC 202**. This block contains two sub-components: **MEMORY ACCESS LOGIC 202A** and **WAVELET TRANSFORM(S) 202B**.

Figure 2

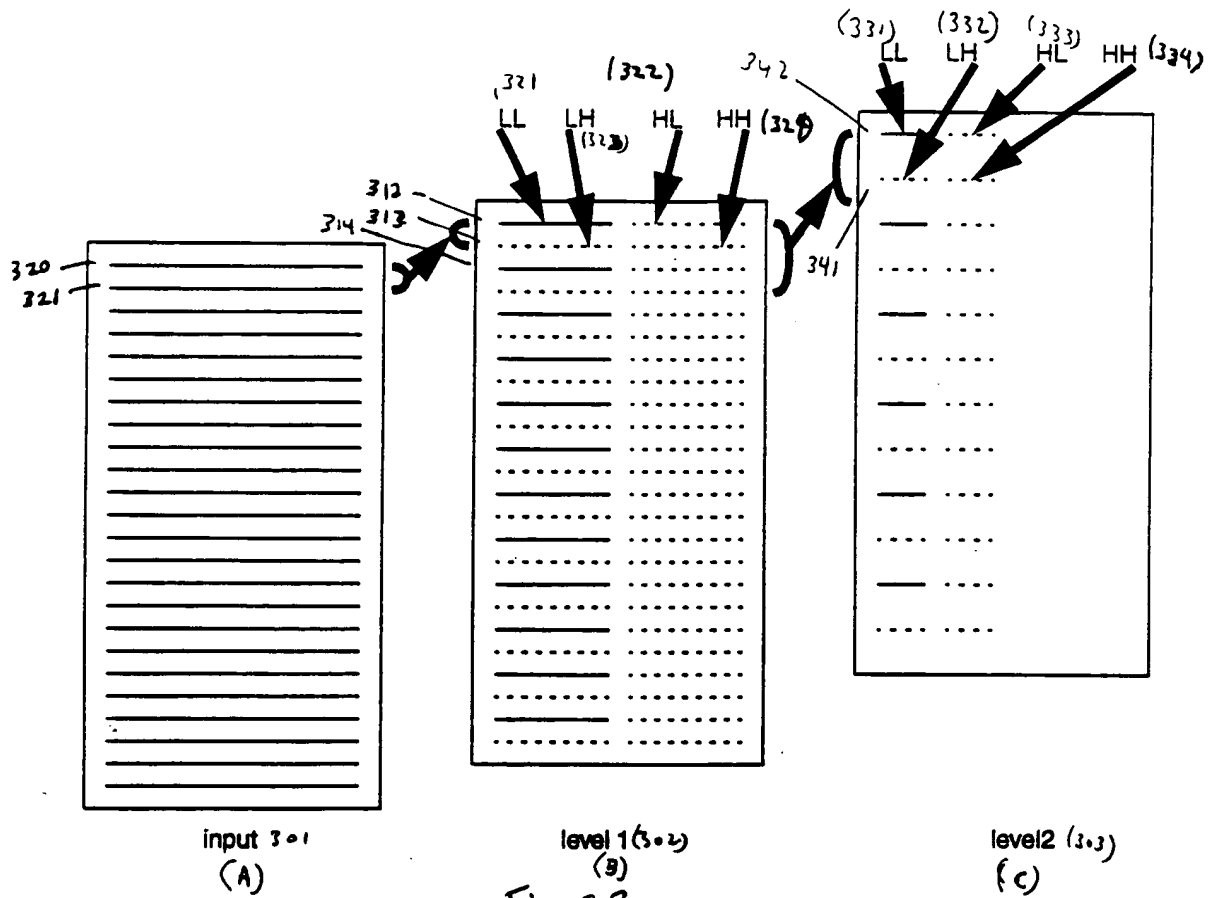


Figure 3

1993-1994

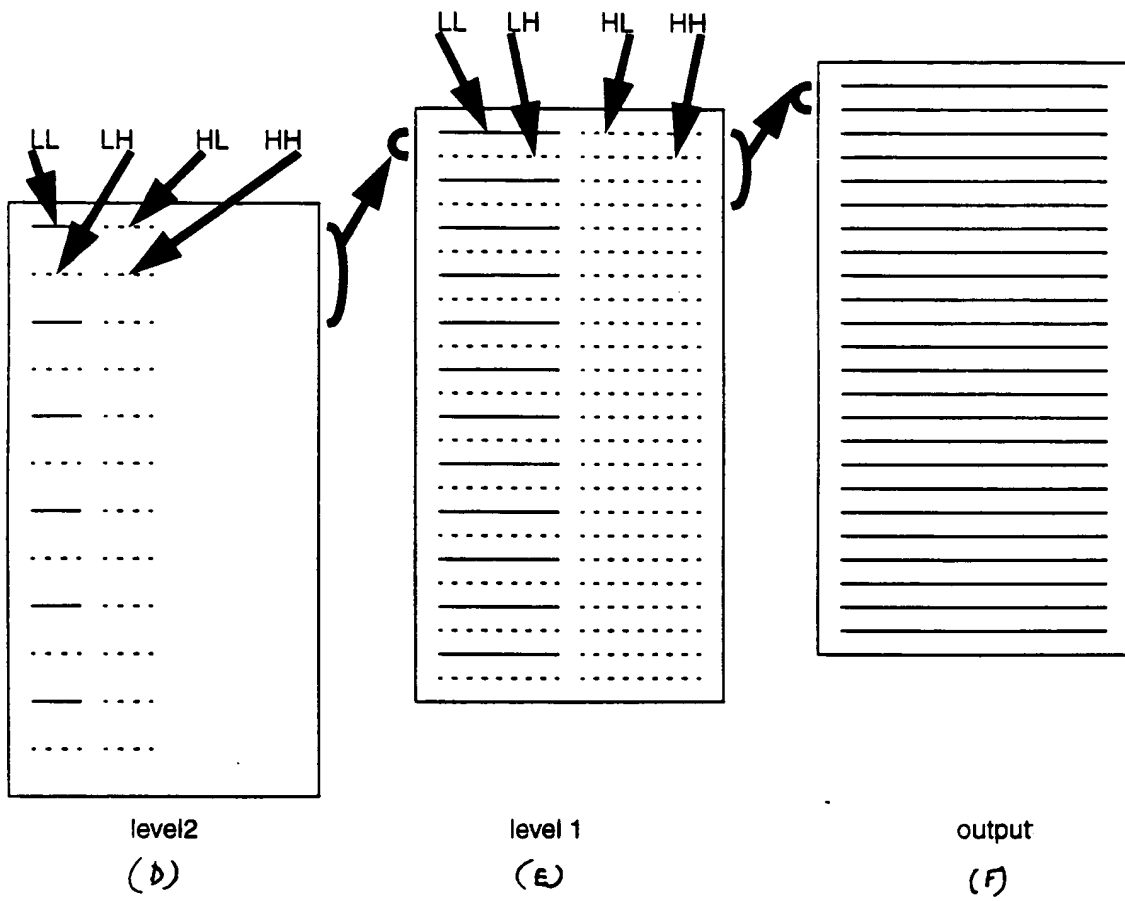


Figure 3

[illegible]

Figure 4 A

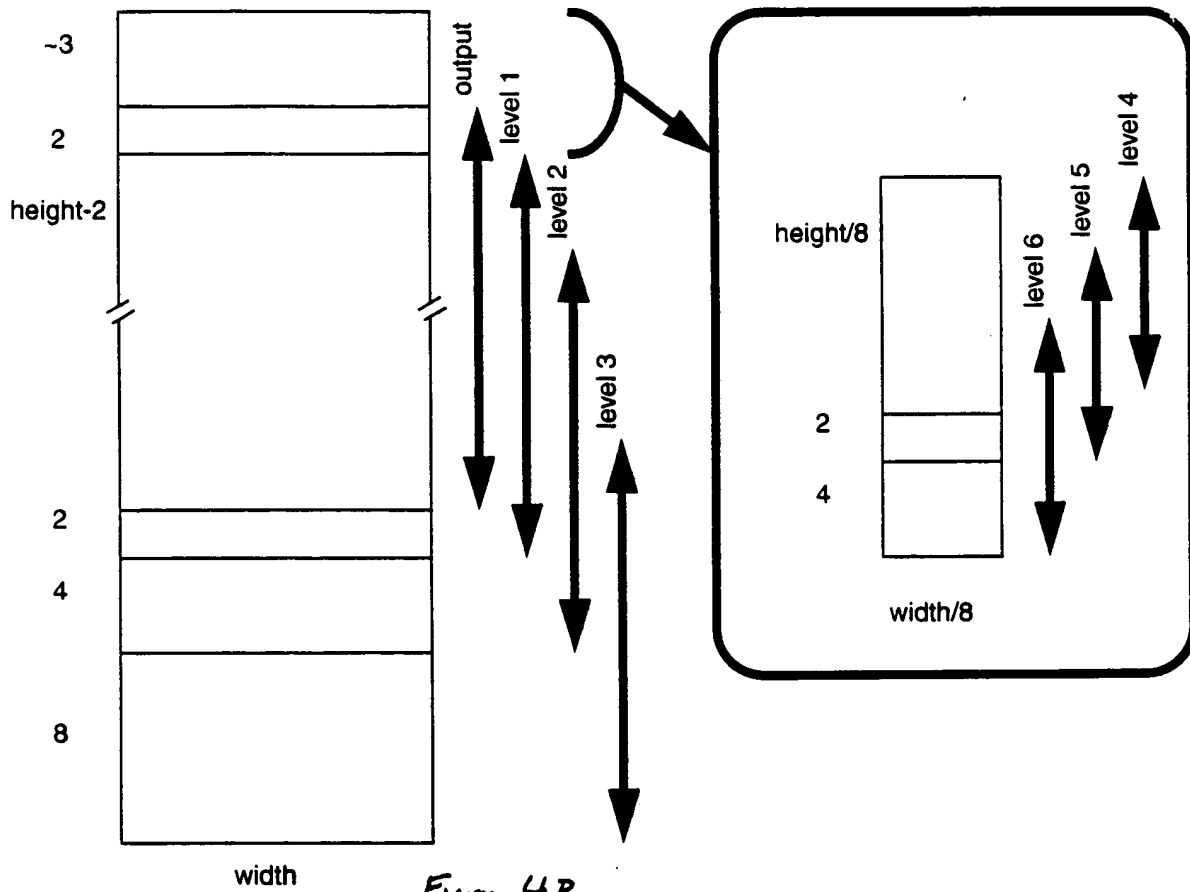


Figure 4B

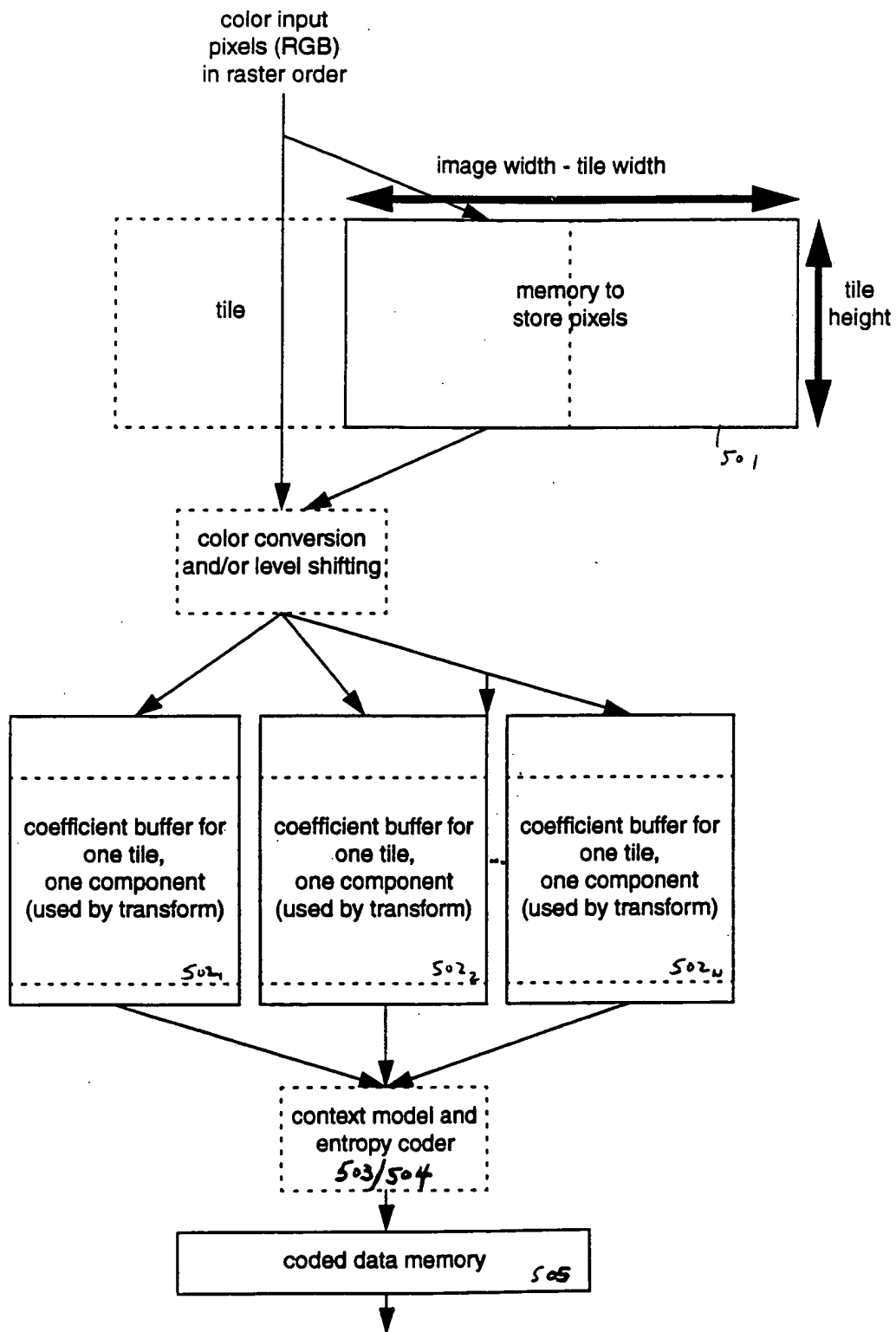
[illegible]

Figure 5

0000384 00000

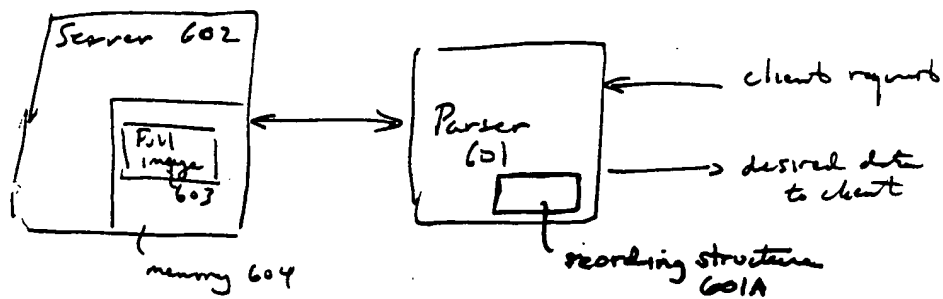


Figure 6A

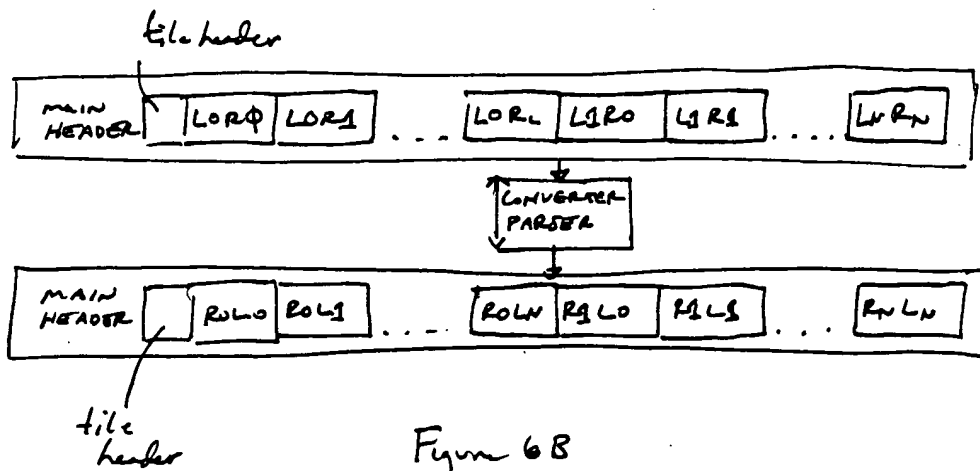


Figure 6B

```

graph TD
    L((L)) <--> RL((RL))
    L <--> RP((RP))
    L <--> CP((CP))
    L <--> PC((PC))
    RL <--> RP
    RL <--> CP
    RL <--> PC
    RP <--> CP
    RP <--> PC
    CP <--> PC
  
```

```

graph TD
    L --> RL
    L --> RP
    RL --> J(( ))
    RP --> J
    J --> CP
    J --> PC
  
```

Figure 7B

FIG. 15670660

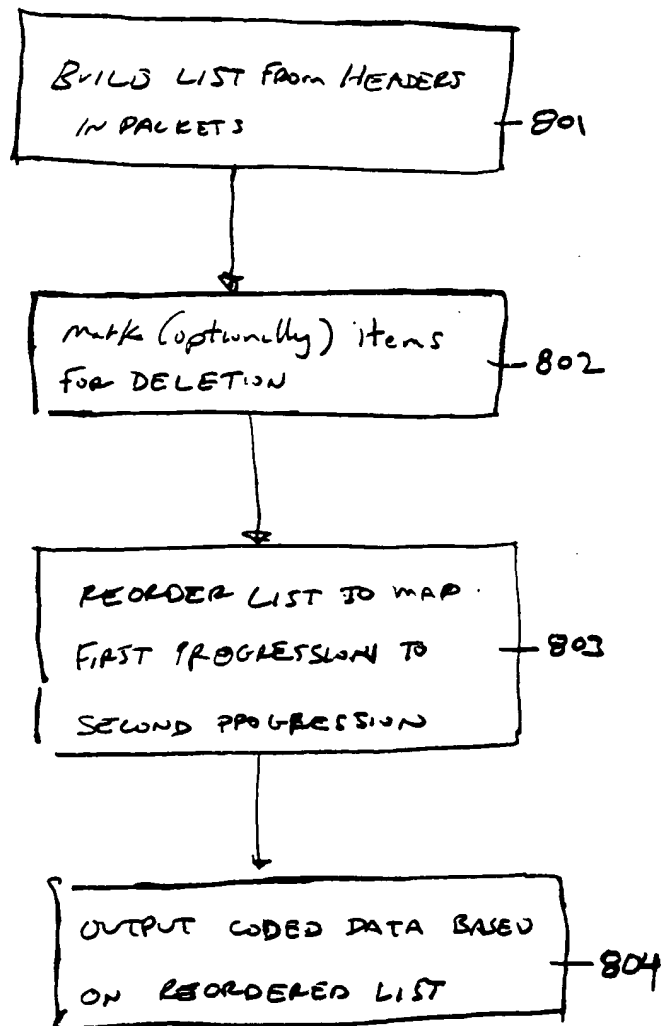


Figure 8

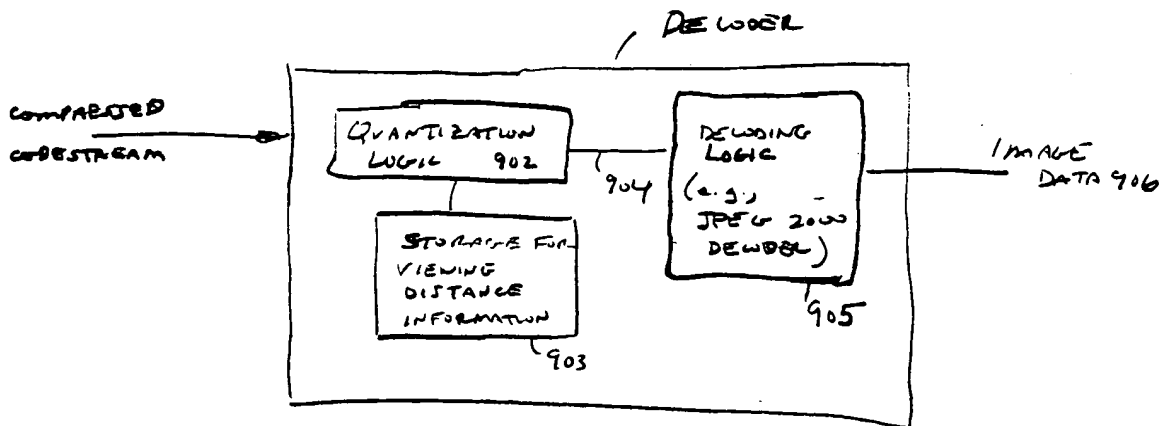


Figure 9

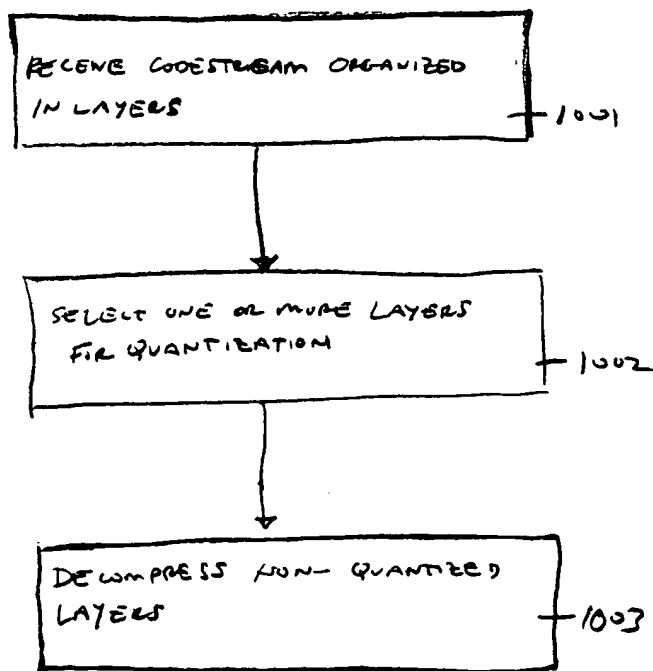


Figure 10

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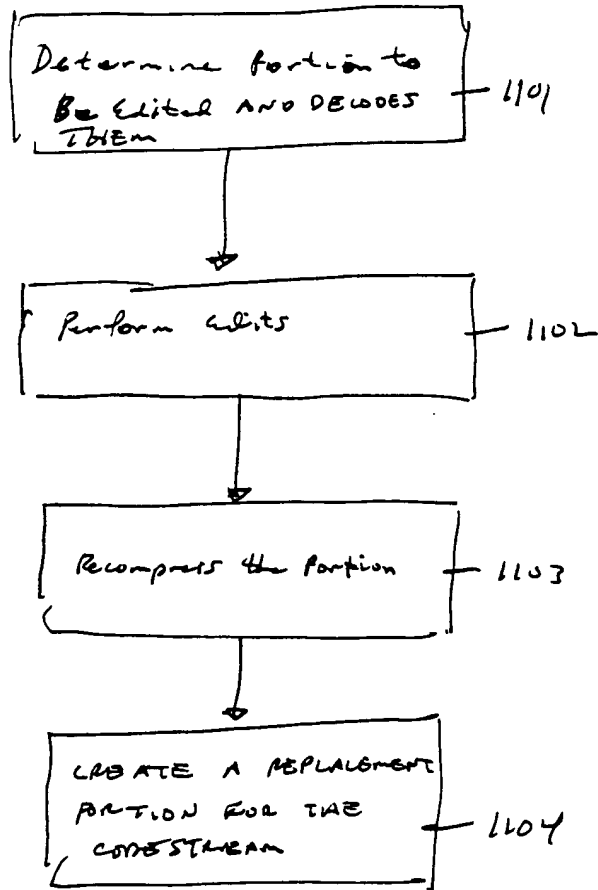
[illegible]

Figure 11

00001331 082001
000000 13310000

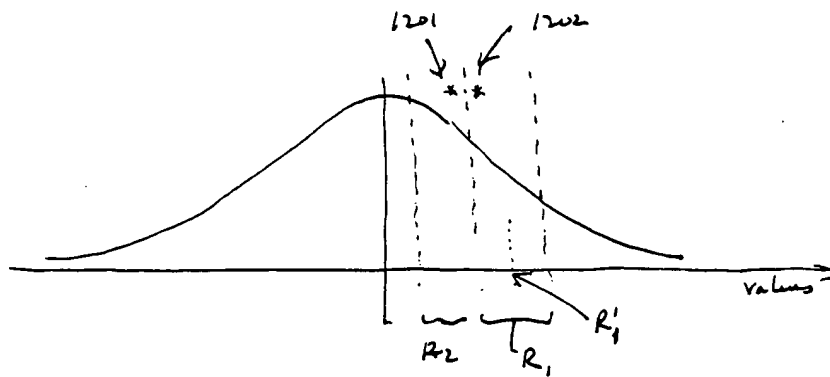


Figure 12

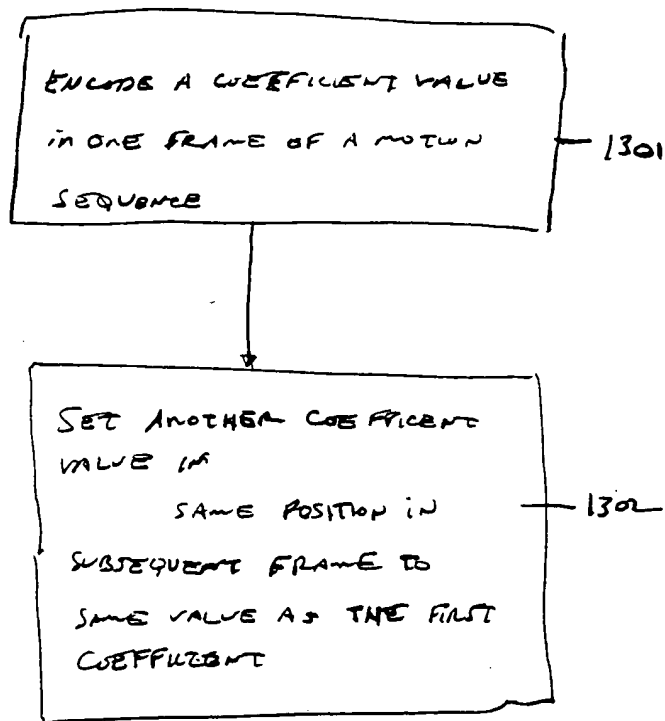
[illegible]

Figure 13

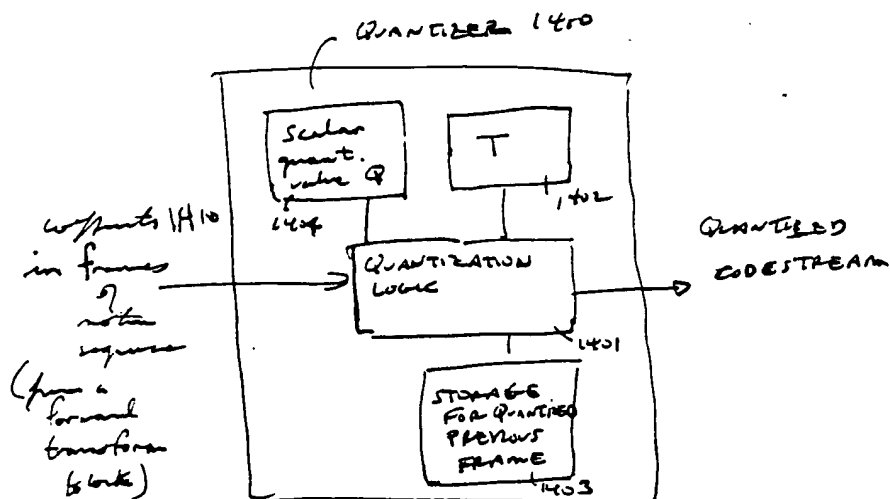


Figure 14

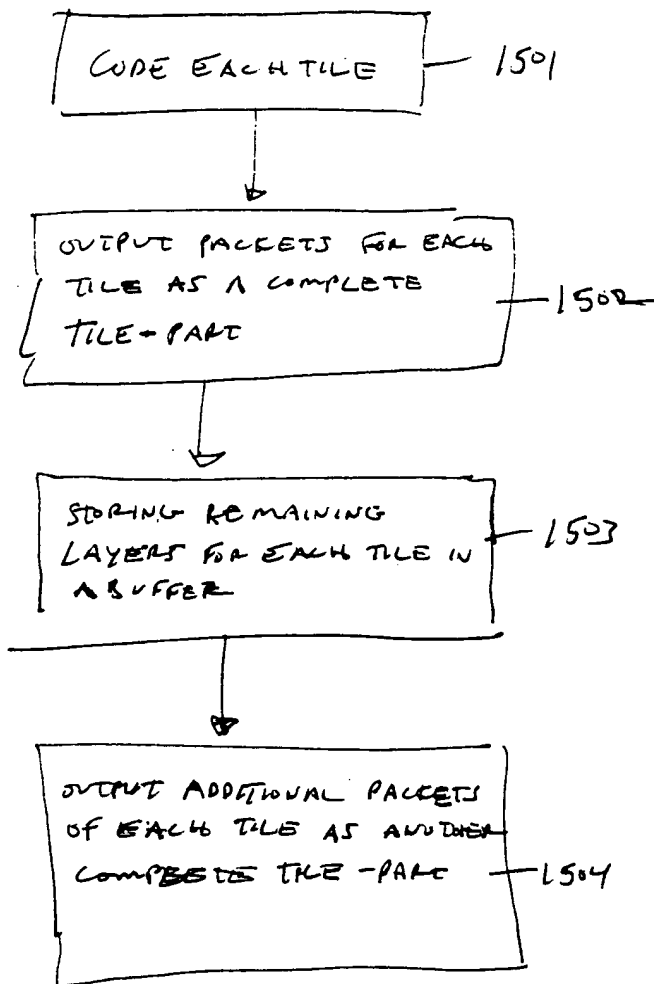


Figure 15 A

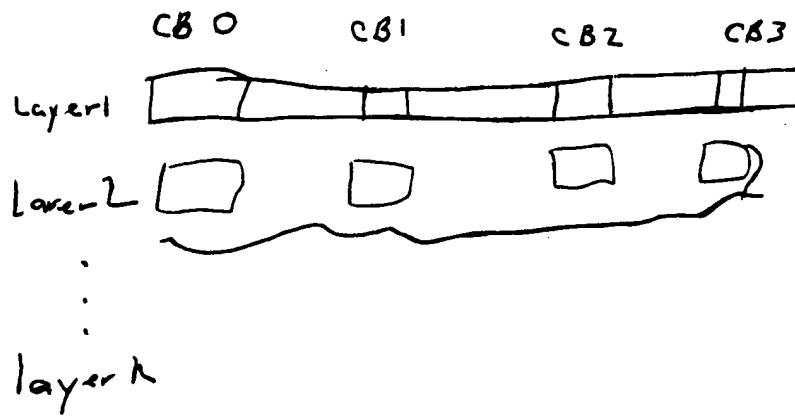
[illegible]

Fig 15B

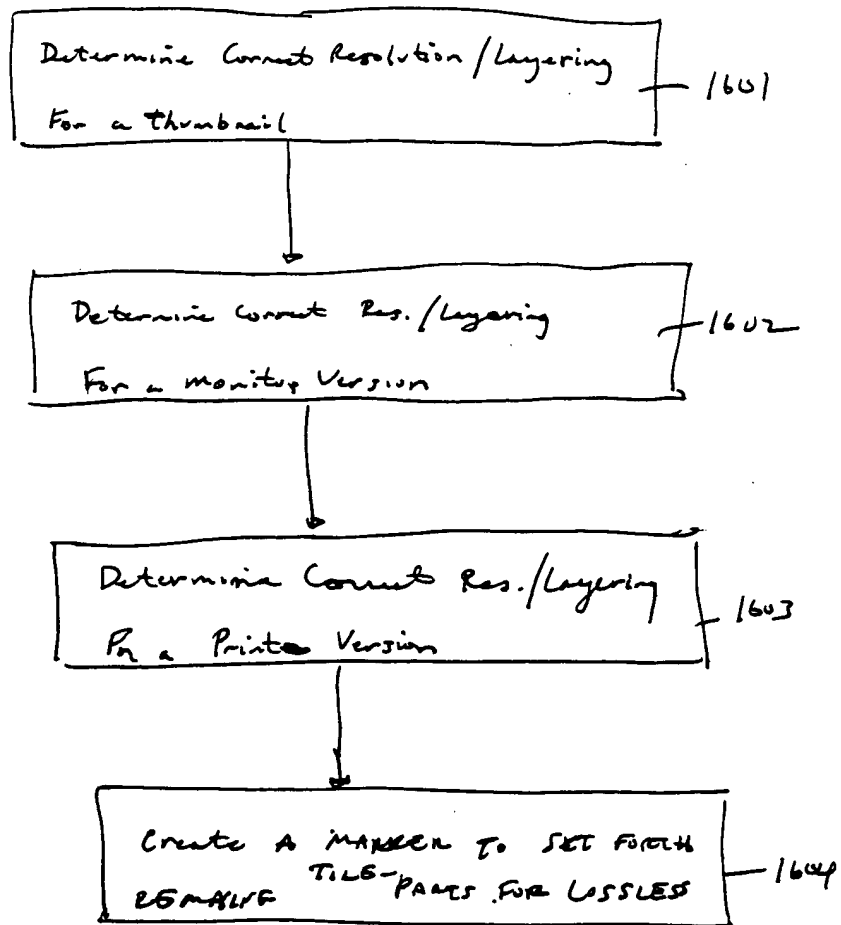


Figure 16

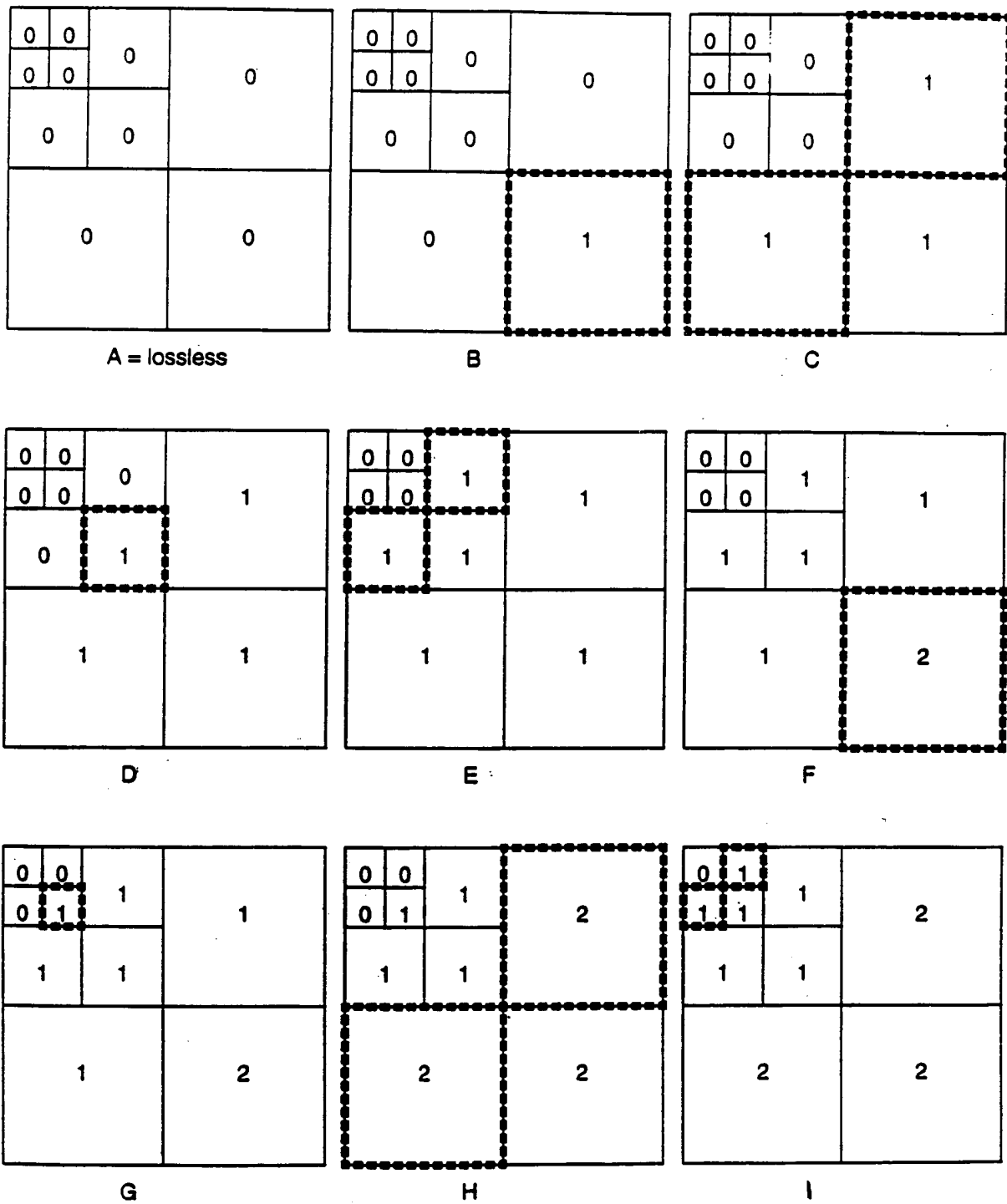


Figure 17

FOUO FOUO FOUO

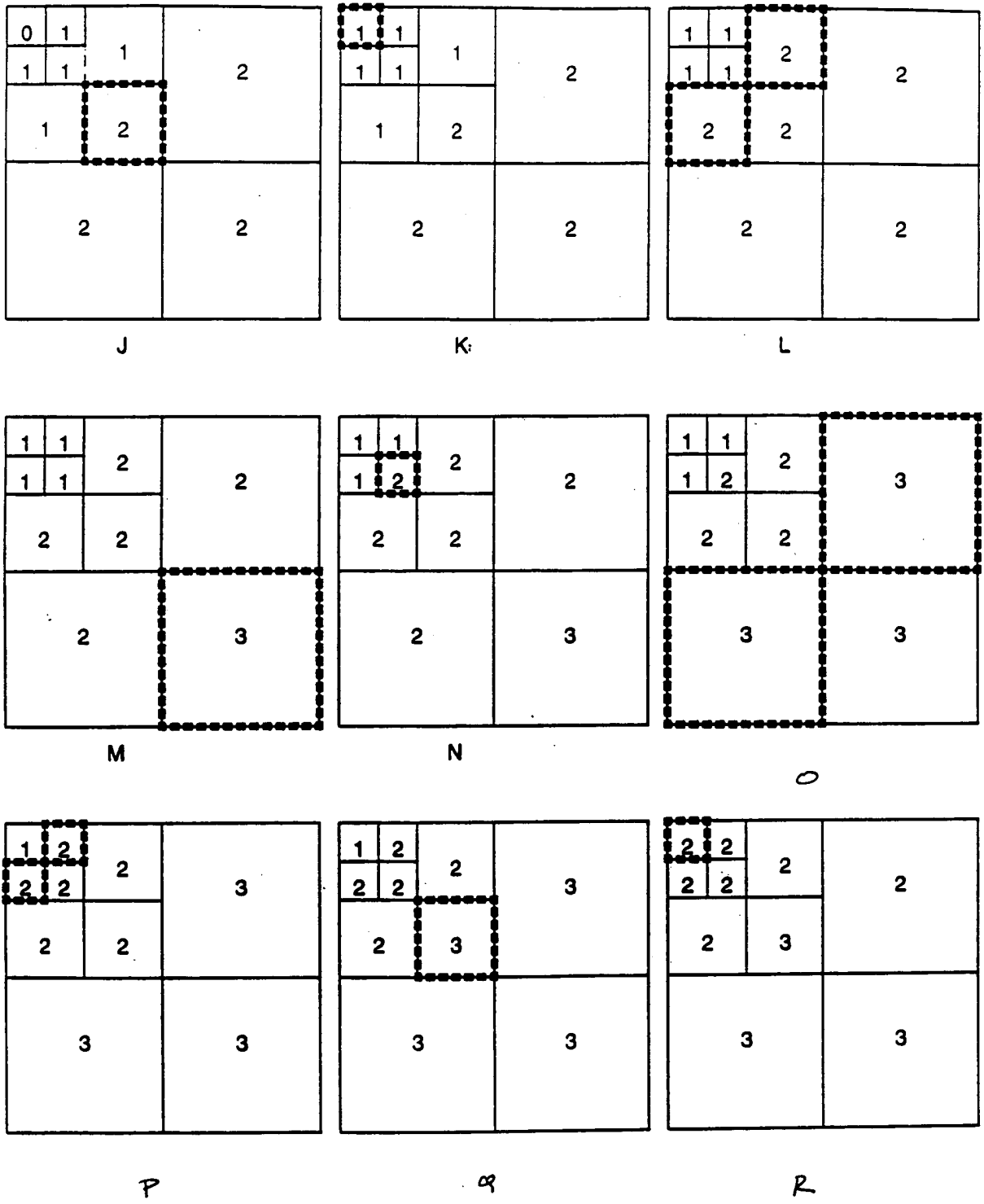


Figure 18

FOUO FFF F0500

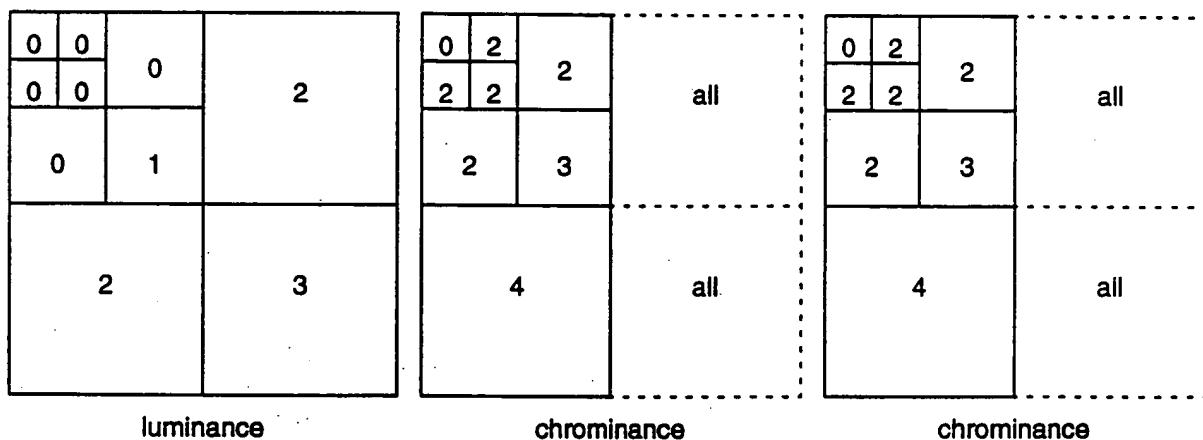


Figure 11

2000

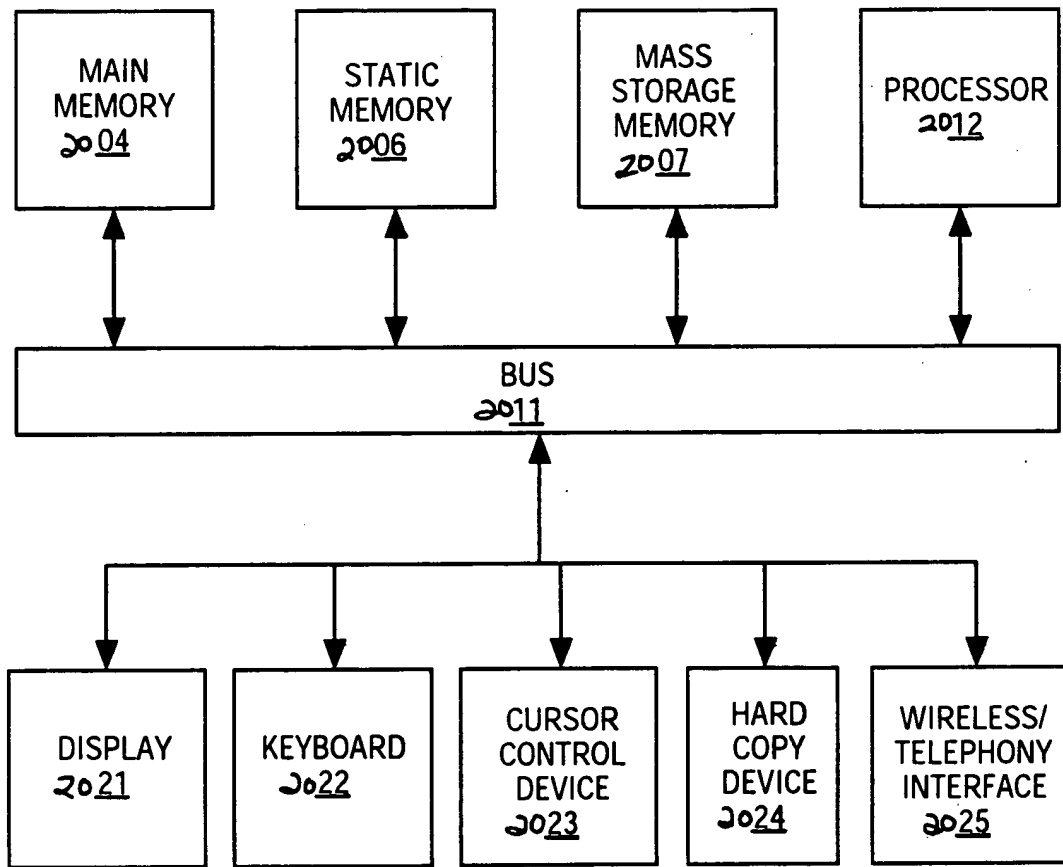


FIG. 20

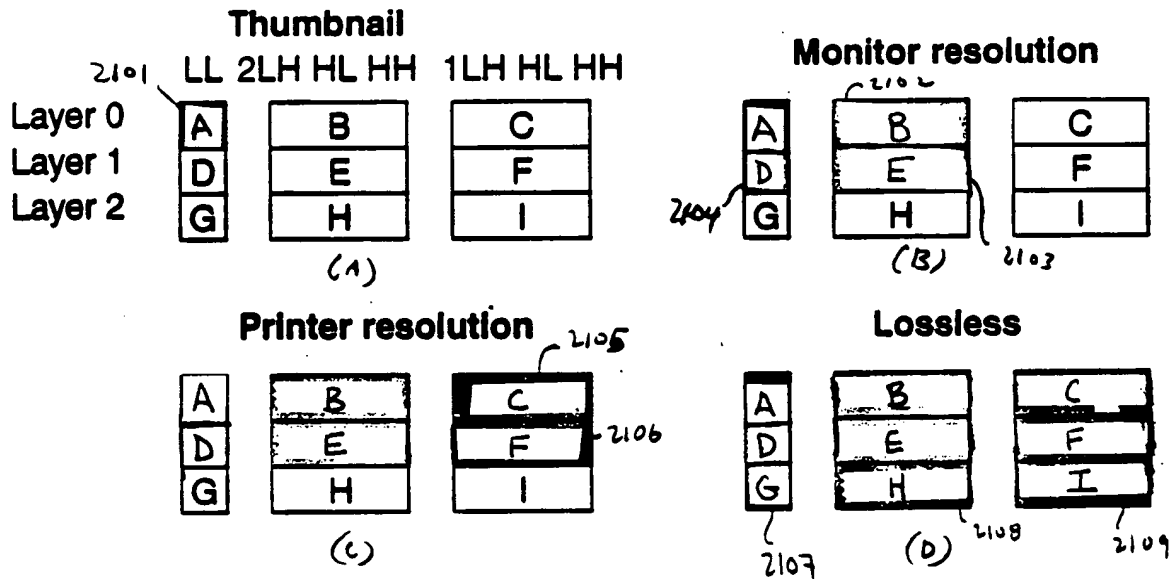


Figure 21

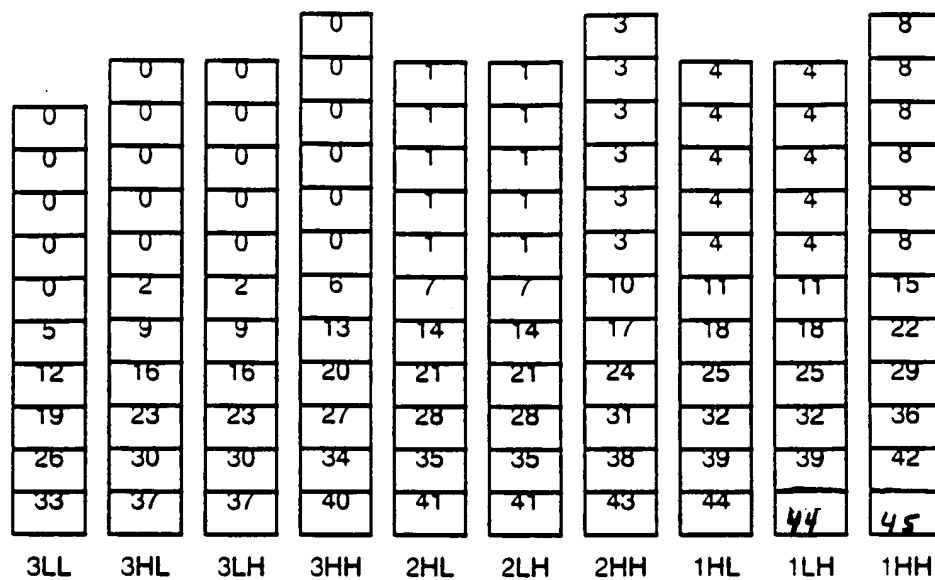


Figure 22

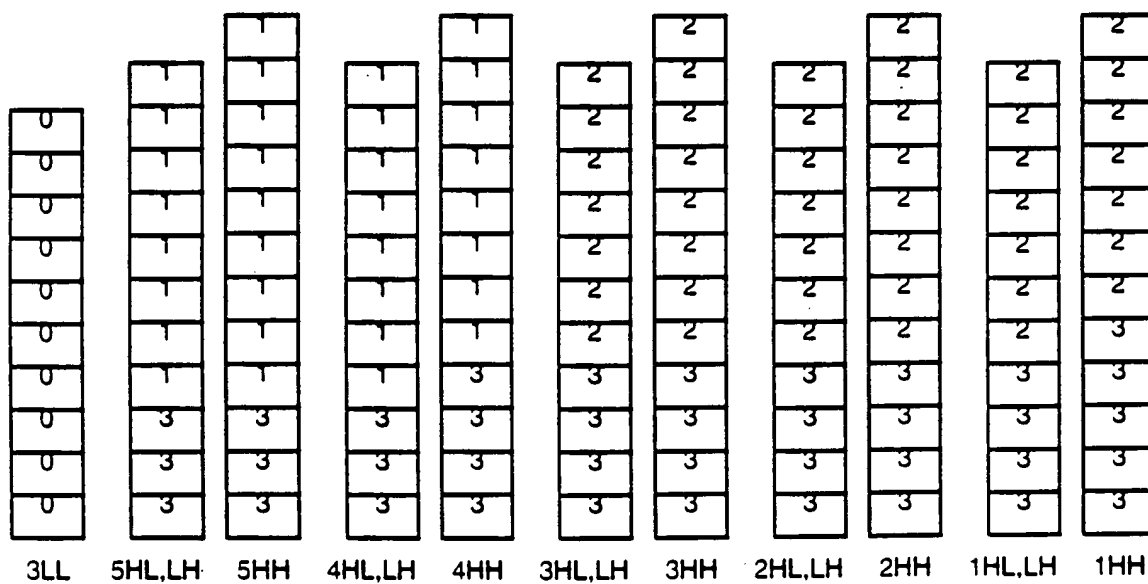


Figure 23

FOUO-1357030

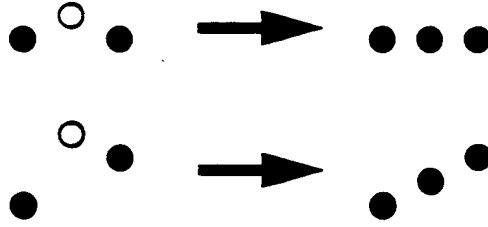


Fig 24

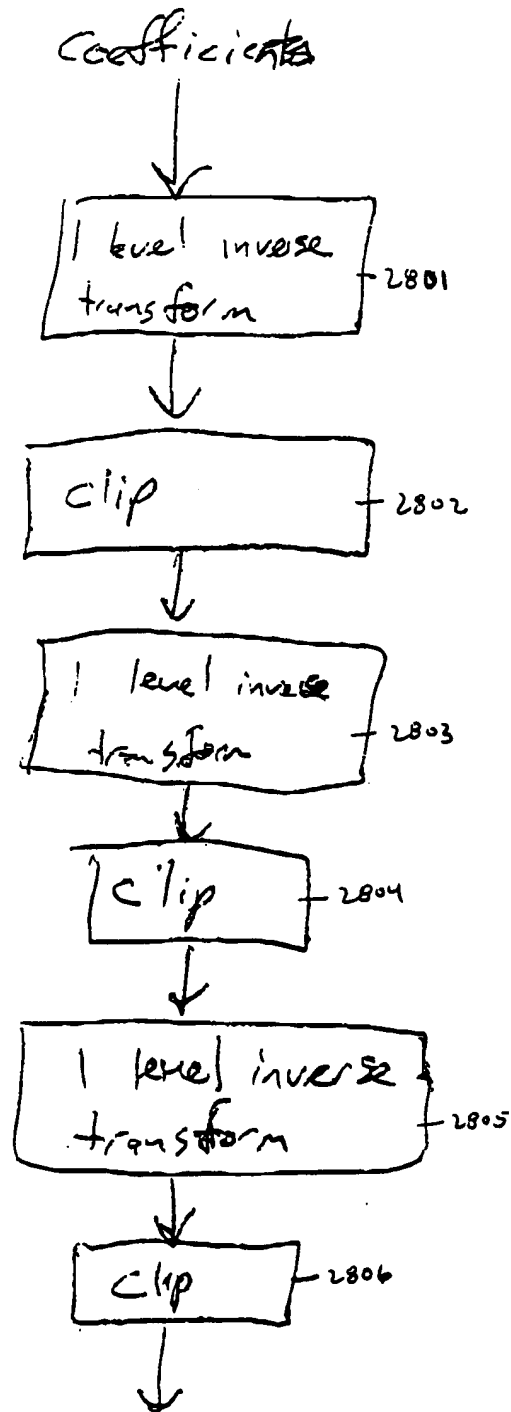
[illegible]

Figure 28